1   Introduction

1.1   Goal of the experimental lab

Aim of this lab is:

- o   Measure the electrical parameters of logic gates,
- o   Verify differences between different logic families.

1.2   Modules and instruments

The circuits to be measured are pre-assembled; during the lab they should only be connected to the instrument tools (power supply, signal generator and oscilloscope) at the measuring points.

The module to be used is named A6 CIRCUITI LOGICI.

1.3   Measurements

For each measurement only one of the pre-assembled circuits on the board is used, arranged according to the suggested configuration.

Note

This experimental lab uses active circuits (i.e. circuits requiring power supply). Use a supply voltage of 5V, derived from one of the tunable voltage outputs of the power supply.

Even if the logic circuits on the board are provided with protection circuits at their input, **always check the amplitude of the signal provided by the external generator BEFORE connecting it to the circuit**.
Remember that external voltages outside the range provided by the voltage supply (ground-5 V in this case) could damage integrated circuits.

To avoid damage to the circuit U4, **verify that the switch S10 is in position 1 BEFORE supplying power**.
Bring it in position 2 only when required experience 2.3 [effect of floating inputs].

2   Measurements

2.1   Transcharacteristic and electrical parameters of logic gates

2.1.1   Module set up

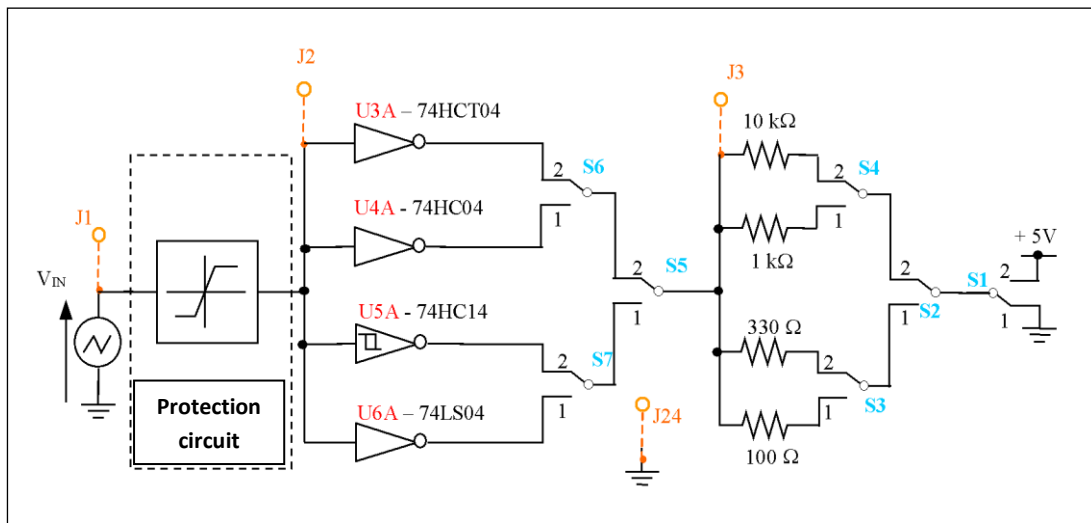Use the module named "Carico Variabile". The circuit to be characterized is reported in Figure 1.

Figure 1: Diagram of the circuit for the measurement of the transcharacteristic.

Table with switch description

Switch	Position on the board	Note
S1	1	Connect output to GND
	2	Connect output to +5 V
S2	1	Select connection towards output of R = 330 Ω / 100 Ω
	2	Select connection towards output of R = 10 kΩ / 1 kΩ
S3	1	Connect towards output R = 100 Ω
	2	Connect towards output R = 330 Ω
S4	1	Connect towards output R = 1 kΩ
	2	Connect towards output R = 10 kΩ
S5	1	Connect U5A and U6A to the load
	2	Connect U3A and U4A t the load
S6	1	Connect U4A to the load
	2	Connect U3A to the load
S7	1	Connect U6A to the load
	2	Connect U5A to the load

2.1.2   Measurements

As for all circuits with power supply, remember to feed first the integrated circuit, then apply the input signal. Use a supply voltage of 5 V (see notes at the beginning of this guide).

Load the gapes with a resistance of 10 kΩ connected towards ground (switches S1=1, S2=2, S4=2,).

2.1.2.1   Measurement of the output levels
1. Adjust the signal generator in such a way that it produces a square wave between 0 V and 5 V (offset = 2.5 V, amplitude = 5 V) at the frequency of 1 kHz. **After checking with the oscilloscope that the signal is correct**, connect the output of the generator to the input of the logic gates (J1).
2. Connect the oscilloscope channel 1 to the input of the logic gates (J2) and the channel 2 to the output (J3). With the oscilloscope in standard mode (Y, t), verify the presence of input and output signals.
3. Check the output waveform of the inverters of the families HCT04, HC04, and LS04 (select the gate on which to perform measurements by setting the switches S5, S6 and S7) and measure the output levels in the H and L states.

2.1.2.2   Transcharacteristic
1. Adjust the signal generator in such a way that it produces a triangular waveform with frequency of 1 kHz and voltage between 0 V and 5 V (offset = 2.5 V and amplitude = 5 V). **After checking with the oscilloscope that the signal is correct**, connect the output of the generator of the input logic gates (J1).
2. Connect the oscilloscope channel 1 to the input of the logic gates (J2) and the channel 2 to the output (J3). With the oscilloscope in standard mode (Y, t), verify the presence of input and output signals.
3. Set the oscilloscope in XY mode (**for analog oscilloscopes lower the brightness of the screen to avoid burning the phosphors of the CRT**).
4. Display the Vo (Vi) transcharacteristics of the logic gates HCT04, HC04, and LS04 (select the gate on which to perform measurements by setting the switches S5, S6 and S7).
5. Record on quoted charts the observed waveforms.
6. Identify and discuss the differences between the gates transcharacteristics.

2.1.2.3   Effects of voltage supply
1. Change the power supply (remaining in the 3 V - 6 V range) and see how the transcharacteristics of the inverters of the different families change.

2.1.2.4   Output voltage-current characteristic
At first perform all the measurements proposed here only for the HC gate with the output at H state, repeat the measurements for the output L state of the LS gate (operations indicated in [] below) after completing all the following steps in the tutorial.

1. Reset the nominal voltage supply (5 V), and reset the oscilloscope in (y, t) mode. Apply a square wave signal with levels outside the range V_{IH}, V_{IL} (and such that they do not damage the components).
2. Refer to the original scheme of section 2.1 and Figure 2. Alternately connecting the 4 output resistors (operating on the switches S2, S3 and S4), obtain the graph $V_O(I_O)$ for the H state [for the L state] of the gates HC04 [LS04] (interpolate the behavior from the 4 measured values). For the L state, connect the resistors to +5 V, for the H state connect them to GND (selector S1) as shown in Figure 2 (right). Calculate the current I_O as the ratio between the voltage drop on pull-up or pull-down resistance and the value of the resistance itself.
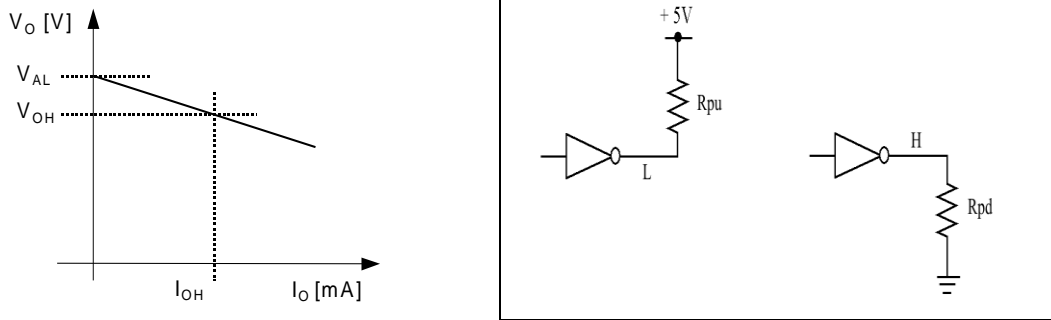
Figure 2: V_{OH} and I_{OH} definition (left) and possible connections of the load (right)

From the Data Sheet one has V_{OH}=4.5 V for the 74HC family and V_{OL}=0.5 V for the 74LS family. Derive the corresponding values of the currents I_{OH} and I_{OL} from the measured output characteristics.

2.2 Characteristics of Open Collector and Totem Pole gates

2.2.1 Module conficuration

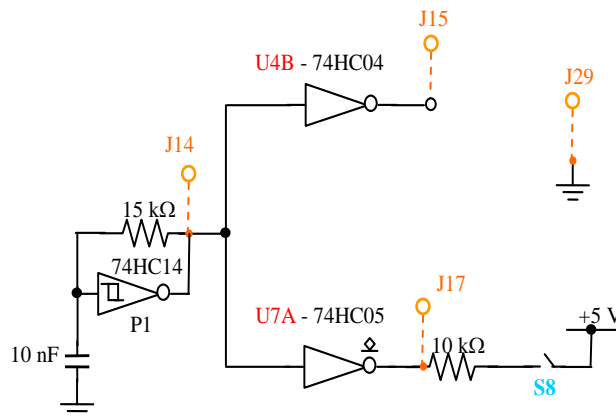The circuit to be measured is reported in Figure 3.

Figure 3: Circuit for the characterization of Open Collector and Totem Pole gates

Switch table

Switch	Position on the board	Note
S8	1	10 kΩ resistance not connected to +5 V
	2	10 kΩ resistance connected to +5V

2.2.2 Measurements

For these measurements it is not necessary to use the signal generator as the input is generated directly from the NOT gate UC5 connected so as to obtain an oscillator, which is an astable circuit that generates a square wave with a frequency of about 10 kHz (see the waveform on the test point J14).

1. Hold the switch S8 open and check the difference between the waveform observed at the outputs of the various logic gates (J15 and J17 test points).
2. Check that the output of the Open Collector gate U7A does not go to a correct voltage level for the H state. Touch with a finger the output of the gate so as to inject a noise and note that for the L state, the output voltage goes to a correct value, while in the H state the output remains open, and then it collects the noise from the environment or external contacts.
3. Close the switch S8 so as to connect the resistor 10 k Ω to the voltage supply. Check the correct operation of U7A.
4. Compare the rising and falling edges of the gates U4B (Totem Pole) and U5B (Open Collector).

2.3 Effects of floating inputs of logic gates

The inputs of CMOS components have very high impedance, so an open CMOS input sets itself to a voltage which depends on the external electric fields. If this voltage has an intermediate value between V_{IH} and V_{IL} (next to the threshold voltage), the output can take on an intermediate level between V_{OH} and V_{OL} (the model of the output as a switch between V_{AL} and GND is no longer valid). In these conditions, the circuit can absorb a current also very high, and dissipate powers such as to damage it. For this reason, never leave CMOS inputs disconnected. It is appropriate that the condition of open input suggested hereafter for the component 74HC04 is maintained only for a short time (less than a minute).

The inputs of logic bipolar gates left open lead themselves to the H (1) state. In this case there is no risk of damage to the component, but you still need to connect the input to an appropriate level to ensure the proper functioning of the system.

What described in the following paragraphs 4 and 5 is justified by a laboratory experience, but must be avoided on a real circuit. Touching the inputs of an integrated circuit, one applies a static voltage (also very high), which can permanently damage the circuit. This applies to all circuits, the CMOS is the most delicate and must be handled with greater care.

When handling chips and electronic boards, one must avoid applying static discharges. Electrostatic charges may be removed by touching the metal chassis or other parts in mass of the system in which the board is inserted, or placing the integrated circuit on a conductor connected to ground, and touching this plane before picking up the component. In any case, by manipulating the electronic components, it is appropriate to avoid touching directly the pins.

Warning

The oscilloscope probe has an equivalent impedance of 10 MΩ. If connected to a CMOS gate, it connects it to ground (logic L state) through this impedance. To perform the following observations of sections 3, 4 and 5, the input must be really open, so DO NOT connect the probes to the input port.

2.3.1 Module configuration

To avoid damage to the circuit U4, put S10 in position 1 BEFORE applying power. Bring it in position 2 only in sections 3, 4 and 5 of the measures. Bring it back in position 1 once the measures are concluded. The measurements must be performed using the gates shown in Figure 4
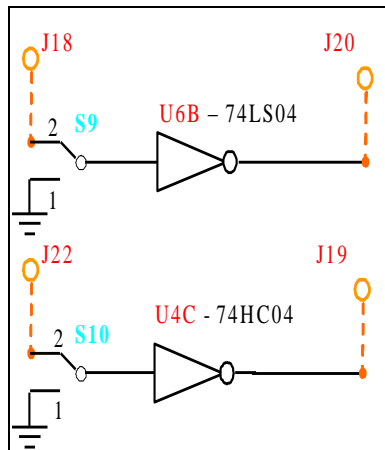
Figure 4: Circuits for the test of the effect of floating gates

Switchtable

Switch	Position on the board	Note
S9	1	Input of U6B to GND
	2	Input of U6B to J18 (open)
S10	1	Input of U4C to GND
	2	Input of U4C to J22 (open)

2.3.2 Measurements

1. Connect the gates to GND (S9 = S10 = 1) and make sure you have the outputs to logic 1.
2. Switch the inputs on J18 and J22 and connect to the inputs a wire with length of about 20 cm.
3. Leave the wire disconnected (floating) and check the effect on the outputs (J20 and J19):
   a. Prendere tra le dita l'estremità libera del filo e con l'altra mano toccare prima V_{CC}, poi GND. Analizzare e giustificare i diversi comportamenti riscontrati.
   b. Take between the fingers the free end of the wire and with the other hand first tap V_{CC}, GND then. Analyze and justify the different behaviors observed.
   c. Pass a charged body (plastic pen rubbed on a cloth) near the inputs and note what happens at the output. Do not touch the terminals to avoid damaging the components. Justify the different behavior of the two outputs.

3 Draft for the final report

Electronic lab 3: Characterization of digital circuits

Date:

3.1.1 Group ....; components:

First name	Last name	Signature

3.1.2 Used instruments

Instrument	Make and model	Characteristics
Waveform generator		
Oscilloscope		
Power supply		
Pre-assembled circuit board		

3.1.3   Synthetic description of the lab goals

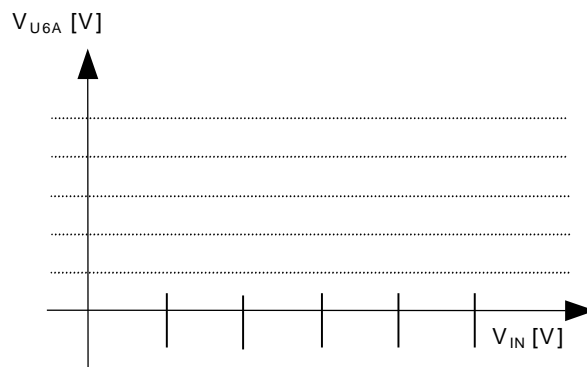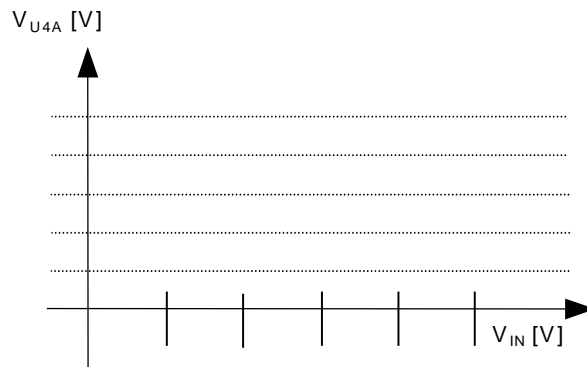## 3.1   Measurements results

3.1.1   Measurement of the electrical parameters and transcharacteristics of logic gates

H and L state levels for the logic families HCT (U3A), HC (U4A), LS (U6A).

Transcharacteristics measured in X-Y mode

V_{U4A} [V]

V_{IN} [V]
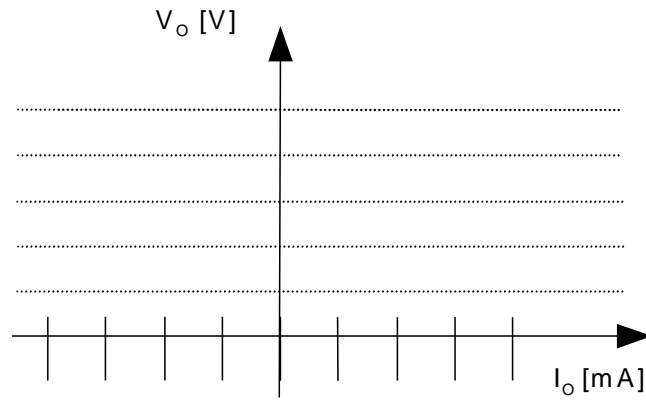
V_{U6A} [V]

V_{IN} [V]
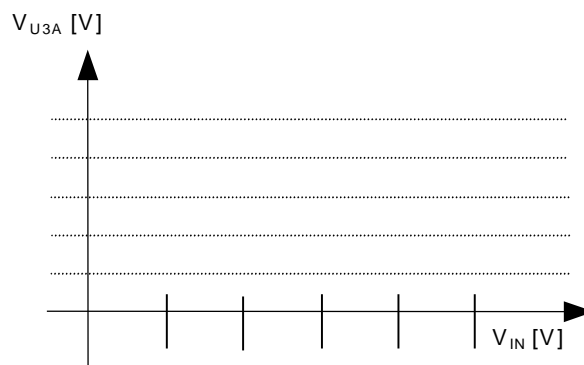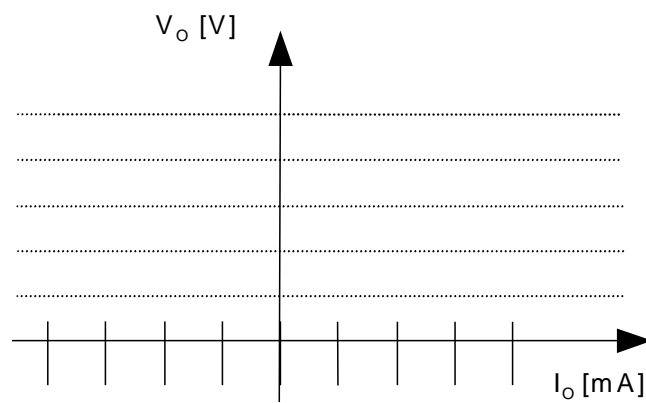
Differences between the different gates.

Changes due to the variation of the voltage supply.

$V_O(I_O)$ graph of the gate U4A

$V_O(I_O)$ graph of the gate U6A

Extracted I_{OH} and I_{OL} values

Effect of different loads on V_{OH} and V_{OL}.

3.1.2 Measurement of *Open Collector* and *Totem Pole* gates.

Difference between the observed waveforms for the various logic gates on the test points J15 e J17.

Discussion on the behavior of the output of the *Open Collector* gate.

Comparison of the rising and falling edges of U7A and U4B.

3.1.3   Study of the effect of *floating* inputs on the output of various logic gates

Effect of floating wire. Discussion.

Inputs connected to V_{CC} and then GND using your fingers. Different behavior observed and their explanation.

Charged body next to the inputs. Explain the behavior of the outputs.